Claims

[c1] 1. A programmable memory controller, comprising:
a main memory controller for sending a request signal when thesaid programmable memory controller needs to accessed data from a memory unit;
a command decoder for decoding thesaid request signal to produce a plurality of command signals;
a cycleperiod setting device for decoding a control signal to produce a cycleperiod setting signal, wherein thesaid control signal controls the maintenance period of thesaid command signal;
a command-sequencing device for ordering and outputting thesaid command signals according to the command signals and thesaidcycleperiod setting signals; and
a command signal output device for receiving thesaid ordered command signals and thesaidcycleperiod setting signals, and controlling thesaidoutput of ordered command signals outputted to the memory during thesaid maintenance period, according to indications provided by thesaidcycleperiod setting signals.

[c2] 2. The memory controller of claim 1, wherein thesaid memory is a synchronous dynamic random access memory (SDRAM).

[c3] 3. The memory controller of claim 1, wherein thesaid memory is a double data rate dynamic random access memory (DDR DRAM).

[c4] 4. The memory controller of claim 1, wherein thesaid maintenance period is set according to the travel distance of thesaid command signal.

[c5] 5. The memory controller of claim 4, wherein thesaid travel distance includes trace length between thesaid control chipset of thesaid memory controller and thesaid memory slot pin of thesaid memory.

[c6] 6. The memory controller of claim 4, wherein thesaid maintenance period can be a first period or a second period, such that thewherein thefirst period command signal is up forrepresents as one clock cycle, if the command signal has a first period and the second period command signal is up for two cycles if the command signal has a second periodrepresents astwoclock cycle.

[c7] 7. The memory controller of claim 6, wherein thesaid maintenance period is the first period if thesaid travel distance is lower than a pre-defined distance and the second period and thesaid maintenance period is the second period if thesaid travel distance exceeds thesaid pre-defined distance.

[c8] 8. The memory controller of claim 7, wherein thesaid pre-defined distance is about 2500 mils.

[c9] 9. A memory access structure having a programmable memory controller therein, wherein thesaid memory access structure controls a plurality of command signals for accessing data inside a memory unit, comprising:
a control chipset having a built-in programmable memory controller, wherein thesaid control chipset controls thesaid maintenance period of thesaid command signals output from thesaid programmable memory controller when thesaid control chipset needs to access data inside thesaid memory unit; and
a memory slot for receiving thesaid command signals and transferring thesaid command signals to the memory unit, wherein thesaid maintenance period of thesaid command signals is determined according to the control signals, and thesaid maintenance period is set according to the distance between thesaid memory controller and thesaid memory slot.

[c10] 10. The memory access structure of claim 9, wherein thesaid programmable memory controller further comprises:
a main memory controller for sending out a request signal when thesaid control chipset needs to access data within thesaid memory unit;
a command decoder for decoding thesaid request signal and reading out thesaid command signals;
a cycleperiod setting device for producing a cycleperiod setting signal according to the control signal, wherein thesaid control signal controls the maintenance period of thesaid command signal;
a command-sequencing device for ordering and producing new command signals according to incoming command signals and thesaidcycleperiod setting signals; and
a command signal output device for controlling thesaid maintenance period of

thesaid ordered command signals going outputted to the memory slot according to indications provided by thesaidcycleperiod setting signals.

[c11] 11. The memory access structure of claim 9, wherein thesaid memory is a synchronous dynamic random access memory (SDRAM).

[c12] 12. The memory access structure of claim 9, wherein thesaid memory is a double data rate dynamic random access memory (DDR DRAM).

[c13] 13. The memory access structure of claim 9, wherein thesaid maintenance period is set according to the travel distance of thesaid command signal.

[c14] 14. The memory access structure of claim 13, wherein thesaid travel distance includes trace length between thesaid control chipset and thesaid memory slot pin position.

[c15] 15. The memory access structure of claim 14, wherein thesaid maintenance period can be a first period or a second period such that thesaid command signal is up for one cycleperiod if thesaid command signal has a first period and thesaid command signal is up for two cycles if thesaid command signal has a second period.

[c16] 16. The memory access structure of claim 14, wherein thesaid maintenance period is the first period if thesaid travel distance is lower than a pre-defined distance and the second period and thesaid maintenance period is the second period if thesaid travel distance exceeds thesaid pre-defined distance.

[c17] 17. The memory access structure of claim 15, wherein thesaid maintenance period is the first period if thesaid travel distance is lower than a pre-defined distance and the second period and thesaid maintenance period is the second period if thesaid travel distance exceeds the pre-defined distance.

[c18] 18. The memory access structure of claim 16, wherein thesaid pre-defined distance is about 2500 mils.

[c19] 19. A motherboard having a memory unit and a memory controller thereon such that maintenance period for command signals traveling fromthesaid memory

controller to the memory unit is determined by their distance of separation, thesaid motherboard comprising:

a memory slot for receiving command signals and sending thesaid command signals to the memory plugged into thesaid memory slot, wherein thesaid maintenance period of thesaid command signal is set according to a control signal, and thesaid maintenance period is related to the distance of separation between thesaid memory controller and thesaid memory slot;

a memory controller, comprising:

a main memory controller for sending a request signal when thesaid programmable memory controller needs to access data from a memory unit;

a command decoder for decoding thesaid request signal to produce a plurality of command signals;

a cycleperiod setting device for decoding a control signal to produce a cycleperiod setting signal, wherein thesaid control signal controls thesaid maintenance period of thesaid command signal;

a command-sequencing device for ordering and outputting thesaid command signals according to the command signals and thesaidcycleperiod setting signals; and

a command signal output device for receivingthesaid ordered command signals and thesaidcycleperiod setting signals, and controlling thesaidordered command signal outputted of ordered command signal to the memory during thesaid maintenance period according to indications provided by thesaidcycleperiod setting signal.

[c20] 20. The motherboard of claim 19, wherein thesaid memory is a synchronous dynamic random access memory (SDRAM).

[c21] 21. The motherboard of claim 19, wherein thesaid memory is a double data rate dynamic random access memory (DDR DRAM).

[c22] 22. The motherboard of claim 19, wherein thesaid maintenance period is set according to the travel distance of thesaid command signal.

[c23] 23. The motherboard of claim 22, wherein thesaid travel distance includes trace length between thesaid control chipset of thesaid memory controller and

thesaid memory slot pin position.

[c24] 24. The motherboard of claim 22, wherein thesaid maintenance period can be a first period or a second period,wherein such that the first period represents as command signal is up for one clockcycle if the command signal has a first period , and the second period command signal is up for two cycles if the command signal has a second periodrepresents as two clock cycle.

[c25] 25. The motherboard of claim 24, wherein thesaid maintenance period is the first period if thesaid travel distance is lower than a pre-defined distance and the second period and thesaid maintenance period is the second period if thesaid travel distance exceeds thesaid pre-defined distance.

[c26] 26. The motherboard of claim 25, wherein thesaid pre-defined distance is about 2500 mils.

[c27] 27. A method of controlling the maintenance period of command signals according to travel distance between a memory unit and a memory controller, comprising the steps of:
generating a request signal when data inside thesaid memory unit needs to be accessed;
decoding thesaid request signal to produce a plurality of command signals, wherein thesaid commands signals are sent to the memory unit to initiate data accessing operations;
decoding a control signal to produce a cycleperiod setting signal, wherein thesaid control·signal controls thesaid maintenance period of thesaid command signal;
sequencing and outputting thesaid sequenced command signals according to thesaid input command signals and thesaidcycleperiod setting signals; and
controlling thesaid sequenced command signal outputtedgoing to the memory unit within thesaid maintenance period according to indications provided by thesaidcycleperiod setting signals.

[c28] 28. The method of claim 27, wherein thesaid memory is a synchronous dynamic random access memory (SDRAM).

[c29] 29. The method of claim 27, wherein thesaid memory is a double data rate dynamic random access memory (DDR DRAM).

[c30] 30. The method of claim 27, wherein thesaid maintenance period is set according to the travel distance of thesaid command signal.

[c31] 31. The method of claim 30, wherein thesaid travel distance includes trace length between thesaid control chipset of thesaid memory controller and thesaid memory slot pin position.

[c32] 32. The method of claim 30, wherein thesaid maintenance period can be a first period or a second period,wherein such that the first period command signal is up for represents as one clock cycle,if the command signal has a first period and second period the command represents as signal is up for two clock cycles if the command signal has a second period, andwherein the first period is shorter than the second period.

[c33] 33. The method of claim 32, wherein thesaid maintenance period is the first period if thesaid travel distance is lower than a pre-defined distance and the second period and thesaid maintenance period is the second period if thesaid travel distance exceeds thesaid pre-defined distance.

[c34] 34. The method of claim 31, wherein thesaid pre-defined distance is about 2500 mils.